

Notice of References Cited	Application/Control No. 10/715,716	Applicant(s)/Patent Under Reexamination JONES, ANTHONY MARK	
	Examiner Vuthe Siek	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chen et al., "A New Gate Delay Model for Simultaneous Switching and Its Applications*," DAC 2001, June 18-22, 2001, ACM 1-58113-297-2/01/0006, pp. 289-294.
	V	Conn et al., "Gradient-Based Optimization of Custom Clrcuits Using a Static-Timing Formulation," DAC 99, ACM 1-58113-109-7/99/06, pp. 1-7.
	W	Chen et al., "Miller Factor for Gate-Level Coupling Delay Calculation," IEEE, Nov. 2000, pp. 68-74.
	X	Agarwal et al., "Efficient Generation of Delay Change Curves for Noise-Aware Static Timing Analysis," IEEE, March, 2002, pp. 1-7.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.